WHAT IS CLAIMED IS:

- 1. An input/output (I/O) circuit, comprising: an I/O pad;
- a pull-down transistor device having a first protective transistor, said pull-down transistor device coupled to said I/O pad;
- a pull-up transistor device having a second protective transistor, said pull-up transistor device coupled to said I/O pad;
- a first switch coupled to said first protective transistor, said first switch being responsive to a first supply voltage, a second supply voltage, and a reference voltage;
- a second switch coupled to said second protective transistor, said second switch being responsive to said first supply voltage and said reference voltage;
- a first self-bias circuit coupled to said first switch wherein said first self-bias circuit uses a voltage at said I/O pad to bias said first protective transistor when both of said first and second supply voltages are powered off; and
- a second self-bias circuit coupled to said second switch wherein said second self-bias circuit uses said voltage at said I/O pad and an output of said first self bias circuit, to bias said second protective transistor when said first supply voltage is powered off.
- 2. The circuit of claim 1, wherein said pull-down transistor device comprises a driver N-channel Metal Oxide Semiconductor (NMOS) transistor having a source coupled to a low supply voltage, a gate coupled to a pre-driver, and a drain coupled to a source of said first protective transistor, said first protective transistor being an NMOS transistor having a gate coupled to said first self-bias circuit and a drain coupled to said I/O pad; and

wherein said pull-up transistor device comprises a driver P-channel Metal Oxide Semiconductor (PMOS) transistor having a source coupled to a high supply voltage, a gate coupled to a pre-driver, and a drain coupled to a source of said second protective transistor, said second protective transistor being a PMOS transistor having a gate coupled to said second self-bias circuit and a drain coupled to said I/O pad.

- 3. The circuit of claim 2, wherein said pull-up transistor device is constructed on a floating well that is coupled to said second self-bias circuit.
- 4. The circuit of claim 1, wherein said first self-bias circuit comprises:
 - a resistor coupled to said I/O pad;
- a plurality of diode-connected PMOS devices coupled in series and disposed between said resistor and a Bias Mid node; and
- a plurality of diode connected NMOS devices coupled in series and disposed between said Bias_Mid node and ground;

wherein when said first and second supply voltages are powered off, a Bias_Mid voltage at said Bias_Mid node is represented by the following equation: $(nV_{TN}) > Bias_Mid > (V_{PAD} - kV_{TP})$ wherein n is the number of said NMOS devices connected in series, V_{TN} is the threshold voltage of said NMOS devices, V_{PAD} is the voltage at the I/O pad, k is the number of said PMOS devices, and V_{TP} is the threshold voltage of said PMOS devices;

and wherein said Bias_Mid provides said first bias voltage.

- 5. The circuit of claim 1, wherein said second self-bias circuit comprises:
 - a resistor coupled to said I/O pad;
- a plurality of PMOS devices connected in series and disposed between said resistor and a V_{GP1} node; and
- a third switch coupled to said first bias circuit that de-couples said supply voltages and provides Bias_Mid from said first bias circuit to the gate

of the one of said plurality of PMOS devices that is connected to said V_{GP1} node;

wherein when one of said supply voltages is powered off, V_{GP1} is approximately equal to V_{PAD} - kV_{TP} wherein k is the number of said PMOS devices, and V_{TP} is the threshold voltage of said PMOS devices;

and wherein said V_{GP1} provides said second bias voltage.

6. A self-biasing an input/output (I/O) circuit comprising: an I/O pad;

a pull-down transistor device having a first protective transistor, said pull-down transistor device coupled to said I/O pad;

a pull-up transistor device having a second protective transistor, said pull-up device coupled to said I/O pad;

a means for biasing said first and second protective transistors using a plurality of supply voltages; and

a means for biasing said first and second protective transistors when one or more of said plurality of supply voltages are off, using a voltage at said I/O pad.

- 7. The circuit of claim 6 further comprising:
- a floating well on which said pull-up transistor device is fabricated; and

a means for biasing said floating well when one or more of said plurality of supply voltages are off.